TITLE OF THE INVENTION

FIELD EMISSION DEVICE HAVING INSULATED COLUMN LINES AND METHOD OF MANUFACTURE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional of application Serial No. 09/383,331, filed August 26, 1999, pending.

Field of the Invention

[0002] The present invention relates generally to flat panel displays and, more particularly, to field emission devices ("FEDs") and methods for manufacturing the same.

Background of the Invention

[0003] As is well known, FED technology operates on the principle of cathodoluminescent phosphors being excited by cold cathode field emission electrons. FIG. 1 is a simplified illustration of a representative portion of a prior art FED 10. In general, the FED 10 comprises a cathode assembly 6 and an anode assembly 8 separated from each other by spacers 4.

[0004] The cathode assembly 6 is typically manufactured using conventional photolithographic processes to form successively defined features on a substrate or base plate 12. In general, a conductive emitter electrode structure 14 is first formed on the substrate 12. Next, a resistive layer 15 is deposited over the conductive structure 14. A pattern of spaced-apart conical cold cathode emitter tips or micropoints 18 is then formed on the substrate 12, followed by a dielectric structure 20 and a conductive or extraction grid structure 22.

[0005] The substrate or base plate 12 is typically formed of glass. The conductive structure 14 may be formed of a metal. The micropoints 18 may be constructed of a number of materials such as, e.g., silicon or molybdenum.

[0006] The conductive structure 14 with the covering resistive layer 15 encircles themicropoints 18 of a pixel group (described below). The portions of the conductive structure 14 shown in FIG. 1 are thus electrically connected and form a column line, which is part of an addressable matrix as will be described below.

[0007] The resistive layer 15 comprising, e.g., amorphous silicon, covers the top and sides of the conductive structure 14. As shown, the outer sides of the base of each conical micropoint 18 are in contact with the resistive layer covering the conductive structure 14. The resistive layer 15 separates the conductive structure 14 from the micropoints 18 and helps prevent damage to the tips of the micropoints 18.

[0008] After the micropoints 18 have been formed on the base plate 12, a dielectric layer is deposited over the micropoints 18 and the resistive layer 15. The dielectric layer, which is later formed into the dielectric structure 20, may comprise silicon dioxide or other materials. Next, a conductive layer is deposited over the dielectric layer. This conductive layer, which is later formed into the conductive grid structure 22, may be made from a variety of materials including chromium, molybdenum and doped polysilicon. Then, using a photolithography/etch process, the dielectric layer and the conductive layer are etched to form the dielectric and conductive grid structures 20, 22, respectively, which surround, but are spaced away from, the micropoints 18 as shown in FIG. 1.

[0009] The conductive grid structure 22 forms a low potential anode that is used to extract electrons from the micropoints 18. The conductive grid structure 22 has a grid construction comprising multiple row lines that are orthogonal to the column lines formed by the conductive structure 14. The row and column lines are part of the addressable matrix as described below.

[0010] The anode assembly 8 usually has a transparent (e.g., glass) substrate 24 and a transparent conductive layer 26 formed over the substrate 24 (on the side facing cathode assembly 6). A black matrix grill 25 is formed over the conductive layer 26 to define pixel regions 28, in which a cathodoluminescent coating is deposited.

[0011] The anode assembly 8 is typically manufactured using conventional photolithography processes to form successively defined features on the lower (as shown in FIG. 1) surface of the transparent substrate 24, starting with transparent conductive layer 26. The next features usually formed are the spacers 4, which project downwardly (e.g., about 150 microns) from conductive layer 26. The black matrix grill 25 is then formed defining the pixel regions 28, in which phosphor material is deposited.

[0012] When assembled, the anode assembly 8 is positioned a predetermined distance

from the cathode assembly 6 (and from micropoints 18) by the spacers 4.

[0013] A power supply 30 is electrically coupled to the conductive layer 26 of the anode assembly 8 and to the conductive structure 14 (at the base of the micropoints 18) and the conductive grid structure 22 of the cathode assembly 6. A vacuum in the space between cathode assembly 6 and anode assembly 8 facilitates travel of electrons emitted from the micropoints 18 towards the pixel regions 28 to impact the pixel regions 28. The emitted electrons strike the cathodoluminescent coating in the pixel regions 28, which emits light to form a video image on a display screen formed by the anode assembly 8.

[0014] The visible display of the FED 10 is normally arranged as a matrix of pixels, one of which (single pixel 32) is shown in FIG. 1. Each pixel in the display is typically associated with a group of micropoint emitters, with all emitters in a group being dedicated to controlling the brightness of their associated pixel. For example, FIG. 1 shows a single pixel 32, with the pixel being associated with micropoints 18. For convenience of illustration, FIG. 1 shows a line of four emitters as being associated with the single pixel 32. Pixel 32 could be a single pixel of a black and white display or a single red, green, or blue dot associated with a single pixel of a color display.

[0015] The row lines of the conductive grid structure 22 and the column lines of the emitter conductive structure 14 form an addressing matrix for selectively activating pixels. Normally, the row and column lines are arranged so that the emitters associated with one pixel can be controlled independently of all other emitters in the display and so that all emitters associated with a single pixel are controlled in unison. In operation, a row signal activates a single conductive row line within the conductive grid structure 22, while a column signal activates a conductive column line within the emitter base conductive structure 14. At the intersection of an activated column and an activated row, a grid-to-emitter voltage differential sufficient to induce field emission will exist, causing illumination of a respective pixel.

[0016] Conventional photolithography processes are typically used to fabricate the various structures (e.g., the conductive structure 14) of the FED 10.

[0017] It has been found in prior art FEDs that the addressing conductive structure 14 sometimes electrically shorts to the conductive grid structure 22. Such electrical shorting degrades the quality of the display and can even make the FED 10 inoperative. The shorting is

believed to result from manufacturing flaws in FEDs. For example, intrinsic defects in the dielectric structure 20 may effectively form conductive paths between the column addressing line and the grid. In addition, variations in the substrate and grid surfaces that cause the surfaces to be closer than intended may also cause shorting. A need, therefore, exists for an improved FED construction that significantly reduces the possibility of electrical shorting between column and row lines.

Brief Summary of the Invention

[0018] The present invention is directed to an FED that has a cathode assembly containing an improved addressing column line structure. The addressing column line structure includes a conductive structure formed on a substrate. A resistive layer is formed over the conductive structure and an insulator layer is formed partly over the resistive layer. Electrical contact between the base of the emitter tips and the addressing column line is achieved through lateral sides of the conductive structure not covered by the insulator layer. The insulator layer helps reduce the possibility of electrical shorts between the column line and the row line structure of the cathode assembly. The insulator layer on top of the addressing column line will allow the use of a thinner subsequent dielectric layer. This thinner dielectric layer, which supports the grid, will provide a lower RC time constant and help achieve better video rate operation. The thinner dielectric layer also will result in smaller grid openings above the tips. This will provide for better beam spots and, therefore, better image resolution. The thinner dielectric layer will require less applied voltage to extract electrons from the emitter tips, resulting in lower power consumption for the FED.

[0019] These and other advantages of the present invention will become readily apparent from the following detailed description wherein embodiments of the invention are shown and described by way of illustration of the best mode of the invention. As will be realized, the invention is capable of other and different embodiments, and its several details may be capable of modifications in various respects, all without departing from the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature and not in a restrictive or limiting sense with the scope of the application being indicated in the claims.

Brief Description of the Drawings

[0020] For a fuller understanding of the nature and objects of the present invention, reference should be made to the following detailed description taken in connection with the accompanying drawings wherein:

[0021] FIG. 1 is a cross-sectional view of a portion of an exemplary prior art FED;

[0022] FIG. 2 is an enlarged cross-sectional view of a part of an FED in accordance with the invention, which illustrates a portion of an insulated addressing column line and also the lateral contact between the base of the emitter tips and the addressing column line; and

[0023] FIG. 3 is a perspective view of a portion of the FED partly broken away to illustrate the inventive addressing column line structure in greater detail.

Detailed Description of the Preferred Embodiments

[0024] The present invention is directed to an improved FED, in which column addressing lines are insulated to reduce the possibility of shorting and to provide other benefits. FIGS. 2 and 3 show a small portion of the cathode assembly of an FED 100 illustrating the inventive column addressing line structure 102.

[0025] The inventive column line structure 102 (a small portion of which is shown) is preferably formed on a substrate or base plate 104 of the cathode assembly. The column line structure 102 comprises a conductive layer 106, a resistive layer 108, and an insulator layer 110.

[0026] The conductive layer 106 is preferably formed like the conductive structure 14 of the FED 10 of FIG. 1. It may comprise a variety of conductive materials including metals. For example, the conductive layer 106 may comprise an aluminum layer having a thickness of about 1000 Å.

[0027] The resistive layer 108 is preferably similar to the resistive layer 15 in FIG. 1 in that it covers the top and sides (as shown in the drawings) of the conductive layer 106. The resistive layer 108 may comprise various materials including silicon. For instance, the resistive layer 108 may be boron doped silicon having a thickness also of about 1000 Å.

[0028] The insulator layer 110 has higher resistivity than the resistive layer 108. It is preferably formed to cover just the top of the resistive layer. If the insulator layer 110 also covered an entire side of the resistive layer 108, then the insulator layer 110 might interfere with

electrical communication between the conductive layer 106 and the adjacent emitter 112. Therefore, as shown in FIGS. 2 and 3, insulator layer 110 preferably covers the top and not the sides of the resistive layer 108. However, in an alternative embodiment, the insulator layer 110 could also cover selected portions of the sides of the resistive layer 108.

[0029] The insulator layer 110 may be made of various insulative materials including, e.g., silicon dioxide or silicon nitride. The insulator layer 110 may have a thickness of about 1000 Å. The combination of resistive layer 108 and insulator layer 110 together preferably introduce a substantial amount of resistivity, preferably, in excess of 1 megaohm between conductive layer 106 and the grid 116.

[0030] The insulator layer 110 is to assist in reducing shorts between the addressing column line and the row lines on the grid 116. The dielectric layer 114 is used to support the grid 116 above the emitters 112. It is to be understood that the insulator layer 110 and the dielectric layer 114 may be made of the same or different material and still be within the scope of the present invention. Regardless of whether the same or different materials are used, as will be discussed below, the insulator layer 110 and the dielectric layer 114 are preferably separately formed. The insulator layer 110 reduces the possibility of shorting between the addressing column line structure and the row line structure, which as previously discussed may result from, e.g., intrinsic defects in the dielectric structure or unintended variations in spacing between the substrate and grid surfaces.

[0031] It should be recognized that a variety of alternative materials of different thicknesses may be used for the conductive layer 106, the resistive layer 108, and the insulator layer 110.

[0032] The improved addressing line structure 102 is preferably fabricated as follows. First, the conductive layer 106 is formed on the base plate 104 using conventional photolithography techniques. Specifically, a layer of material from which the conductive layer 106 is to be formed is first deposited on the base plate 104 using conventional deposition techniques. Then, using a conventional photolithography/etch/strip sequence, the conductive layer 106 is formed.

[0033] Thereafter, the resistive and insulator layers 108, 110 are formed. First, a layer of material from which the resistive layer 108 is formed is deposited over the conductive

layer 106. Then, a layer of material from which the insulator layer 110 is formed is deposited over the layer of resistive material. Next, using a conventional photolithography/etch/strip sequence, the resistive layer 108 and insulator layer 110 are formed on the conductive layer 106.

[0034] To complete fabrication of the cathode assembly, the micropoint emitters 112, the dielectric layer 114, and the conductive grid 116 are then formed preferably using conventional photolithography techniques. The micropoint emitters 112 are preferably formed such that the addressing line structure 102 is disposed around (and in contact with) adjacent micropoint emitters 112 associated with a given pixel. The insulating layer deposited over the resistive layer 108, which covers the conductive layer 106, does not affect the electrical relationship between the conductive layer 106 and the adjacent emitters 112 because the sides of the addressing line structure 102 in contact with the emitters are not insulated.

[0035] The cathode assembly formed with the inventive column addressing line structure can be assembled with a conventional anode assembly like that shown in FIG. 1 to form an FED.

[0036] Adding the insulator layer 110 to the addressing lines requires one additional deposition step in FED fabrication, namely the step of depositing the insulator layer 110 on top of the resistive layer 108. However, no extra photolithography sequences are required for forming the insulator layer 110 because the insulator and resistive layers 110, 108 are etched from a single mask pattern. This is possible because when viewed from the top, in the preferred embodiment of the addressing line (as shown in FIG. 2), the outer edges of the insulator layer 110 and the underlying resistive layer 108 are substantially aligned, i.e., the insulator layer 110 substantially exactly overlies the resistive layer 108. Therefore, no extra photolithography (or masking) steps are needed, which are well known to be costly, complex and time consuming.

[0037] Many variations of the above-described preferred embodiments are possible. For example, one alternative embodiment might include more layers than the above-described combination of an insulator layer 110 and a resistive layer 108. For example, multiple resistive layers could be layered on top of one another to form a suitably high series resistance.

[0038] It has been found that by insulating column addressing lines in accordance with the invention, there is a significantly reduced possibility of shorting between column and row lines when the FED is in use.

[0039] The insulated column line structure also provides other advantages. For instance, addition of the insulator layer 110 increases the distance between the conductive layer 106 and the grid 116. This improves the FEDs' refresh rate by decreasing the associated RC constant. "R" is the resistance of the conductive lines (both grid and column) and "C" is the capacitance between a column line and the grid layer. C is proportional to A/d (where "A" is a cross-sectional area and "d" is the distance between the plates). By increasing d, C is reduced, which thereby reduces the RC constant. The reduced RC time constant will assist in achieving a better video rate operation of the display.

[0040] Other benefits of the invention include an ability to use thinner dielectric layers 114, which allows smaller cavity openings around the emitter tip to be constructed. This consequently reduces the beam spot and improves display images.

[0041] Having described embodiments of the present invention, it should be apparent that modifications can be made without departing from the scope of the present invention.